AMENDMENTS TO THE CLAIMS

1. (Previously presented) A pixel cell comprising:

a first conversion pinned photodiode that generates charge;

a second pinned photodiode that generates charge;

a first transistor between the first and second pinned photodiodes for transferring charge generated by the first pinned photodiode to the second pinned photodiode; and

readout circuitry that provides first readout signals indicating charge generated by the first pinned photodiode and second readout signals indicating charge generated by the second pinned photodiode.

2-3. (Canceled).

4. (Previously presented) The pixel cell of claim 1, wherein the second pinned photodiode is a floating diffusion region.

5. (Canceled).

6. (Previously presented) The pixel cell of claim 1, wherein the second pinned photodiode has a higher pinning voltage than the first pinned photodiode.

7. (Canceled).

8. (Previously presented) The pixel cell of claim 1, further comprising a second transistor having a gate coupled to the first pinned photodiode, wherein the second transistor is a shutter transistor for determining an integration time.

9. (Currently amended) The pixel cell of claim 1, wherein the first transistor is coupled to the first and second pinned photodiodes [[is]].

10. (Currently amended) The pixel cell of claim 8, further comprising a doped well in [[the]]a substrate below the second transistor gate.

11. (Previously presented) The pixel cell of claim 1, further comprising at least one doped well in a substrate.

12. (Previously presented) The pixel cell of claim 11, wherein the second pinned photodiode is in the doped well.

13. (Previously presented) The pixel cell of claim 11, wherein the first pinned photodiode is not in the doped well.

14. (Previously presented) The pixel cell of claim 11, wherein the pinned photodiode is not in the doped well.

15. (Previously presented) The pixel cell of claim 14, wherein there is a doped well between the first and second pinned photodiodes.

16. (Previously presented) The pixel cell of claim 1, further comprising a gate of a second transistor electrically connected to the second pinned photodiode, wherein the second transistor is an output source follower transistor.

17-23. (Canceled).

24. (Previously presented) A pixel cell comprising:

a first pinned photodiode that generates charge in response to light;

a second pinned photodiode that generates charge in response to light and receives charge transferred from the first pinned photodiode;

a first transistor coupled to the first and second pinned photodiodes for transferring charge generated by the first pinned photodiode to the second pinned photodiode; and

a gate of a second transistor coupled to the second pinned photodiode.

25. (Previously presented) An image sensor comprising:

an array of pixel cells, wherein at least two pixel cells each comprise:

a first pinned photodiode that generates charge;

a second pinned photodiode that generates charge;

a first transistor between the first and second pinned photodiodes for transferring charge generated by the first pinned photodiode to the second pinned photodiode; and

readout circuitry that provides first readout signals indicating charge generated by the first pinned photodiode and second readout signals indicating charge generated by the second pinned photodiode.

26-28. (Canceled).

29. (Previously presented) The image sensor of claim 25, wherein the second pinned photodiode is a floating diffusion region.

30. (Canceled).

31. (Previously presented) The image sensor of claim 30, wherein the second pinned photodiode has a higher pinning voltage than the first pinned photodiode.

32. (Previously presented) The image sensor of claim 25, further comprising a gate of a second transistor coupled to the first pinned photodiode, wherein the second transistor is a shutter transistor for determining an integration time.

33. (Previously presented) The image sensor of claim 25, wherein the first transistor is coupled to the first and second pinned photodiodes.

34. (Currently amended) The image sensor of claim 32, further comprising a doped well in [[the]]a substrate below the second transistor gate.

35. (Previously presented) The image sensor of claim 25, further comprising at least one doped well in a substrate, wherein the first and second pinned photodiodes are within the substrate.

36. (Previously presented) The image sensor of claim 35, wherein the second pinned photodiode is in the doped well.

37. (Previously presented) The image sensor of claim 35, wherein the first pinned photodiode is not in the doped well.

38. (Previously presented) The image sensor of claim 35, wherein the second pinned photodiode is not in the doped well.

39. (Previously presented) The image sensor of claim 38, wherein there is a doped well between the first and second pinned photodiodes.

40. (Previously presented) The image sensor of claim 25, wherein the at least two pixel cells further comprise a gate of a second transistor electrically connected to

the second pinned photodiode, wherein the second transistor is an output source follower transistor.

41. (Previously presented) The image sensor of claim 25, further comprising control circuitry that applies a criterion to readout signals from the second pinned photodiodes until the criterion is met, and when the criterion is met, causes the readout circuitry to provide signals indicating charge generated by the first pinned photodiode.

42. (Original) The image sensor of claim 25, further comprising correlated double sampling (CDS) circuitry that performs CDS operations.

43. (Canceled).

44. (Previously presented) A processor system, comprising:

a processor;

an image sensor coupled to the processor, the image sensor comprising an array of pixel cells, wherein at least two of the pixel cells each comprise:

a first pinned photodiode that generates charge;

a second pinned photodiode that generates charge;

a first transistor between the first and second pinned photodiodes for transferring charge generated by the first pinned photodiode to the second pinned photodiode;

readout circuitry that provides first readout signals indicating charge generated by the first pinned photodiode and second readout signals indicating charge generated by the second pinned photodiode; and

control circuitry that applies a criterion to readout signals from the second photo-conversion devices until the criterion is met, and when the criterion is met, causes the readout circuitry to provide signals indicating charge generated by the first photo-conversion devices.

45. (Original) The processor system of claim 44, wherein the image sensor further comprises correlated double sampling (CDS) circuitry that performs CDS operations.

46-47. (Canceled).

48. (Previously presented) A method of forming a pixel cell, the method comprising:

forming a first pinned photodiode that generates charge;

forming a second pinned photodiode that generates charge;

forming a first transistor between the first and second pinned photodiodes for transferring charge generated by the first pinned photodiode to the second pinned photodiode; and

forming readout circuitry that provides first readout signals indicating charge generated by the first pinned photodiode and second readout signals indicating charge generated by the second pinned photodiode.

49-51. (Canceled).

52. (Previously presented) The method of claim 48, wherein the act of forming the second pinned photodiode comprises forming a floating diffusion region.

53. (Canceled).

54. (Previously presented) The method of claim 53, further comprising setting a pinning voltage for the second photo-conversion device higher than a pinning voltage for the first photo-conversion device.

55. (Previously presented) The method of claim 48, further comprising forming a second transistor coupled to the first pinned photodiode, wherein the act of forming the second transistor comprises forming a shutter transistor for determining an integration.

56. (Canceled).

57. (Previously presented) The method of claim 55, further comprising forming a doped well of a first conductivity type in a substrate below a gate of the second transistor.

58. (Previously presented) The method of claim 48, further comprising forming at least one doped well of a first conductivity type in a substrate, wherein the first and second pinned photodiodes are formed within the substrate.

59. (Previously presented) The method of claim 58, wherein the act of forming the second pinned photodiode comprises forming the second pinned photodiode in the doped well.

60. (Previously presented) The method of claim 58, wherein the act of forming the first pinned photodiode comprises forming the first pinned photodiode outside of the doped well.

61. (Previously presented) The method of claim 58, wherein the act of forming the second pinned photodiode comprises forming the second pinned photodiode outside of the doped well.

62. (Previously presented) The method of claim 58, wherein the act of forming the at least one doped well comprises forming a doped well between the first and second pinned photodiodes.

63. (Previously presented) The method of claim 48, further comprising forming a second transistor, the act of forming the second transistor comprising forming a gate of an output source follower transistor electrically connected to the second pinned photodiode.

Claims 64-72 (Canceled).